REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 7-11 and 17-20 are present in this application, and are rejected over U.S. 6,401,156 (Mergard et al.) in view of U.S. 5,784,532 (McDonough et al.). Claims 7 and 17 are amended by way of the present amendment.

Claims 9-11 and 18-20 are amended for clarity. For example, claim 9 is amended to more definitely state that an instruction decoder is included in the extension unit, and claims 10-11 are amended since claim 7 does not recite a logic circuit.

The present invention as recited in the pending claims is directed to a processor and a semiconductor integrated circuit. The processor includes a processor core, an extension unit and a direct memory access (DMA) controller. A control bus is connected to both the processor core and the extension unit. The extension unit includes a first execution unit which is a reconfigurable first execution unit. A non-limiting example of such a structure shown in Figure 2, where a processor core 10 is connected to extension unit 32 via control bus CB.

Turning to the 35 U.S.C. § 103(a) rejection, the processor of claim 7 and the integrated circuit of claim 17 are not disclosed or suggested by Mergard et al. combined with McDonough et al. Mergard et al. discloses a flexible microcontroller as shown in Figure 1 having a CPU 36, processor bus 76, programmable interrupt controller (PIC) 48 and general purpose (GP) bus 72. The Office Action asserts that the extension unit of claims 7 and 17 corresponds to PIC 48 and the processor core corresponds to CPU 36. PIC 48 is described in column 6 as including three industry standard programmable interrupt controllers integrated together, and PIC 48 may be programmed to operate in a PC/AT-compatible mode. The Office Action also refers to column 10, lines 1-13 of Mergard et al. where the PICs are described as 8259A programmable interrupt controllers. Mergard et al. does not suggest that

PIC 48 is reconfigurable, and the Official Action provides no evidence that PIC 48 is reconfigurable. The Office Action simply states that the microcontroller M "granted PC/AT functionality of programmable interrupt controller and programmed the PIC functionalities" which only establishes that PIC 48 is programmable. Accordingly, the rejections of claims 7 and 17 are not supported by Mergard et al.

Claims 7 and 17 also recite a control bus connected to both the processor core and the extension unit. As shown in Figure 1, Mergard et al. contains no control bus connected to both CPU 36 (asserted to be the recited processor core) and PIC 48 (asserted to be the extension unit). PIC 48 is connected to GP bus 72 and is not connected to processor bus 76 including the processor control bus. Accordingly, for this additional reason Mergard et al. does not disclose or suggest the processor of claim 7 or the semiconductor integrated circuit of claim 17.

McDonough et al. is relied upon for teaching a processor core having an instruction decoder. Even if such teaching could be combined with Mergard et al., the combination would not suggest the processor of claim 7 or the integrated circuit of claim 17 since neither reference discloses a processor core, a reconfigurable first execution unit and a control bus connected to both the processor core and the extension unit, as recited in claims 7 and 17. Accordingly, claims 7 and 17 are patentable over a combination of Mergard et al. and McDonough et al.

Claim 8 recites the extension unit further comprises an instruction decoder, a control register and local memory. The discussion of claim 8 on page 3 of the Office Action refers to the program controller being an 80XX microprocessor. However, the extension unit was asserted to be PIC 48 which, according to Mergard et al., is an 8259A PIC. Accordingly, Mergard et al. does not disclose or suggest the processor of claim 8. Moreover, the extension unit contains the first execution unit connected to the processor core, and a control bus

connects the processor core and the extension unit. Claim 8 is patentable over a combination of Mergard et al. and McDonough et al.

Claims 9 and 18 recite that the extension unit comprises an instruction decoder which comprises a reconfigurable logic circuit that is the same as the reconfigurable first execution unit. First, Mergard et al. in Figure 2 shows a general PC/AT system, and has no explanation of the details of the configuration of an extension unit. Mergard et al. clearly does not disclose any extension unit having such reconfigurable unit and circuit. Claims 9 and 18 are clearly patentable over a combination of Mergard et al. and McDonough et al.

Claims 10 and 19 recite that configuration data is provided to the reconfigurable first execution unit through data transmission from the DMA controller via a configuration interface connecting the reconfigurable first execution unit in the extension unit and the DMA controller. The Office Action refers to DMAC 22. As explained above, PIC 48 is a programmable device and there is no description in Mergard et al. of sending configuration data to PIC 48 from any source, including DMAC 22. Accordingly, claims 10 and 19 are patentable over a combination of Mergard et al. and McDonough et al.

The processor of claim 11 (dependent from claims 7 and 8) and the integrated circuit of claim 20 (dependent from claims 17 and 18) are not disclosed or suggested by Mergard et al. or McDonough et al. at least for the reasons described above for the respective claims from which they depend. Thus, claims 11 and 20 are also patentably distinguishable over a combination of Mergard et al. and McDonough et al.

It is respectfully submitted that the present application is in condition for allowance, and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

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